ABSTRACT

An addressing mechanism for charging and discharging quasi-capacitive elements in an X-Y matrix. The addressing mechanism may be configured to toggle a resistor-capacitor (RC) time constant between large and small values such as by opening or closing a circuit path to a low impedance resistor disposed in parallel with a higher impedance in-line resistor. When this occurs, elements in the X-Y matrix can be addressed and controlled. The X-Y matrix may be comprised of multiple "rows" and "columns" of conductors where crosstalk may occur along the columns and rows. Crosstalk may be curtailed by using either hysteresis management or global control of the row's impedance along its entire length. The resulting control obviates the need for active devices at each matrix element to perform the switching functions.